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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,058	04/27/2005	Mihai Adrian Tiberiu Sanduleanu	NL02 1079 US	9258

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NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
PEREZ, JAMES M	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
05/29/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/533,058	SANDULEANU, MIHAI ADRIAN TIBERIU	
	Examiner	Art Unit	
	JAMES M. PEREZ	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8 and 9* is/are allowed.

6)☐ Claim(s) *1-3,5 and 6* is/are rejected.

7)☒ Claim(s) *4 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 April 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. In view of the appeal brief filed on 2/5/2009, PROSECUTION IS HEREBY REOPENED. A new ground of rejection set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below

/Shuwang Liu/

Supervisory Patent Examiner, Art Unit 2611

Response to Arguments

2. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claims 1-7 are objected to for the following informalities:

(1) Claim 1, lines 1-2 states a "Phase Locked Loop comprising a frequency detector including an unbalanced quadricorrelator, the quadricorrelator comprising a frequency detector" (emphasis added). Two separate frequency detectors which are introduced as "a frequency detector". The examiner suggests modifying the claim language to better distinguish between the different frequency detectors. Note that such a modification has already been made in clam 8.

(2) Claim 1, line 5 states "a phase detector controlled by a first signal pair provided by the first multiplexer and by a second signal pair provided by the second multiplexer" and claim 7 (which depends from claim 1) states, "a fine control input is controlled by a signal provided by a phase detector coupled to a second charge pump coupled to second low-pass filter" (emphasis added). Two separate phase detectors which are introduced as "a phase detector". The examiner suggests modifying the claim language to better distinguish between the different phase detectors. Note that such a modification has already been made in clam 8.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2 and 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moser (USPN 6,853,696) in view of Sudjian (US 7,409,027).

With regards to claim 1, Moser teaches a Phase Locked Loop (PLL) (fig. 1: col. 1, lines 25-30 and col. 6, lines 12-41: where the clock recovery unit achieves a phase and frequency lock-in condition with the input signal (col. 2, lines 25-35) and therefore is a type of PLL) comprising a frequency detector (figs. 1 and 2: element 10: col. 5, lines 28-34: note that fig. 2 is the circuit diagram schematic illustration of the frequency detector usable in the embodiment shown in fig. 1) including an unbalanced quadricorrelator (fig. 2: col. 7, lines 8-15: note the digital frequency detector in its entirety is an unbalance quadricorrelator, where an unbalance quadricorrelator is a type of frequency detector), the quadricorrelator (fig. 2: col. 7, lines 8-15) comprising a frequency detector (fig. 2: elements 20 and 22: col. 7, lines 29-49: wherein the output signals (labeled FQ1 and FQ2) from the frequency detector give correlative information about a quadrature phase relationship (col. 8, lines 42-52), which is similar to output signals 'PI' and 'PQ' in figure 2 of the instant application) including clocked bi-stable circuits (fig. 2: elements 20 and 22: col. 7, lines 29-49) coupled to a first multiplexer (fig. 2: elements 20 and 22: col. 7, lines 29-49) and to a second multiplexer (fig. 2: elements 20 and 22: col. 7, lines 29-49) being controlled by a signal having a same bitrate as the incoming signal (fig. 2: elements 20, 22, and DATA: col. 7, lines 29-49: note that both D flip-flop (or D latch) pairs and multiplexers are controlled by the incoming data signal as shown in figure 2), and a phase detector (fig. 2: elements 34a and 34b: col. 7, lines 50-63: wherein the

examiner interprets said D flip-flops to be phase detector since elements 34a and 34b are clocked and input FQ1 and FQ2 respectively, where FQ1 and FQ2 give correlative information about a quadrature phase relationship (col. 8, lines 42-52)) controlled by a first signal provided by the first multiplexer (fig. 2: col. 7, lines 50-63: FQ2) and by a second signal provided by the second multiplexer (fig. 2: col. 7, lines 50-63: FQ2).

Moser does not explicitly teach a frequency detector including double edge clock bi-stable circuits and a phase detector controlled by a first signal pair provided by the first multiplexer and by a second signal pair provided by the second multiplexer. (emphasis added)

Sudjian teaches adapting D flip-flops (figs. 3 and 4: elements 22a-22b and 32a-32b) and multiplexers (figs. 3 and 4: elements 22a-22b and 34) to be compatible with differential incoming data signals (fig. 3: signal DATA: col. 5, lines 54-65) and differential quadrature clock signals (fig. 3: elements VCO_0 and VCO_90: col. 5, lines 54-65).

One of ordinary skill in the art at the time of the invention would clearly recognize the benefits of modifying the quadricorrelator of Moser to with the teachings and differential circuitry of Sudjian to yield the predictable benefits and results of implementing frequency detection (using a quadricorrelator) on a differential data signal as opposed to a single-end signal. Specifically, it would have been obvious to modify the known frequency detector circuitry (Moser elements 20 and 22 which are with in the quadricorrelator) with the known differential D flip-flops and differential multiplexers of Sudjian in order to perform similar functions on a differential input data signal and differential quadrature clocking signal to generate differential error signals (where FQ1

and FQ2 are originally single-end signals), where the modified FQ2 and FQ1 are the claimed first and second signal pair, respectively, and the differential D flip-flop pairs clock by differential quadrature clock signal are obviously double edge clock bi-stable circuits, and the relationship between the phase detector (Moser: fig. 2: elements 34a and 34b) and signals FQ1 and FQ2 was previously addressed. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the quadricorrelator (frequency detector) of Moser to with the teachings and differential circuitry of Sudjian to yield the predictable benefits and results of implementing frequency detection (using a quadricorrelator) on a differential data signal as stated above.

With regards to claim 2, Moser in view of Sudjian teaches a Phase Locked Loop as claimed in claim 1, including double edge clock bi-stable circuits above.

Moser teaches the frequency detector comprises a first pair of clocked bi-stable circuits (fig. 2: elements 22, 30a, and 30b: col. 7, lines 29-49) coupled to the first multiplexer (fig. 2: elements 22 and 32: col. 7, lines 29-49), and a second pair of clocked bi-stable circuits (fig. 2: elements 20, 26a, and 26b: col. 7, lines 29-49) coupled to the second multiplexer (fig. 2: elements 20 and 28: col. 7, lines 29-49), which first and second pairs (fig. 2: elements 20 and 22) are supplied by mutually quadrature phase shifted signals (fig. 2: elements 20 and 22, which respectively use quadrature clock signals ICK and QCK) respectively to provide the first signal (fig. 2: FQ2) and the

second signal (fig. 2: FQ1) indicative for a phase difference between the incoming signal and mutually quadrature phase shifted signals (col. 8, lines 42-52).

Moser does not explicitly teach a first pair of double edge clocked bi-stable circuits, a second pair of double edge clocked bi-stable circuits, the first signal pair, and the second signal pair.

Sudjian teaches adapting D flip-flops (figs. 3 and 4: elements 22a-22b and 32a-32b) and multiplexers (figs. 3 and 4: elements 22a-22b and 34) to be compatible with differential incoming data signals (fig. 3: signal DATA: col. 5, lines 54-65) and differential quadrature clock signals (fig. 3: elements VCO_0 and VCO_90: col. 5, lines 54-65).

One of ordinary skill in the art at the time of the invention would clearly recognize the benefits of modifying the quadricorrelator of Moser to with the teachings and differential circuitry of Sudjian to yield the predictable benefits and results of implementing frequency detection (using a quadricorrelator) on a differential data signal as opposed to a single-end signal. Specifically, it would have been obvious to modify the known frequency detector circuitry (Moser elements 20 and 22 which are with in the quadricorrelator) with the known differential D flip-flops and differential multiplexers of Sudjian in order to perform similar functions on a differential input data signal and differential quadrature clocking signal to generate differential error signals (where FQ1 and FQ2 are originally single-end signals), where the modified FQ2 and FQ1 are the claimed first and second signal pair, respectively, and the differential D flip-flop pairs clock by differential quadrature clock signal are obviously double edge clock bi-stable circuits, and the relationship between the phase detector (Moser: fig. 2: elements 34a

and 34b) and signals FQ1 and FQ2 was previously addressed. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the quadricorrelator (frequency detector) of Moser to with the teachings and differential circuitry of Sudjian to yield the predictable benefits and results of implementing frequency detection (using a quadricorrelator) on a differential data signal as stated above.

With regards to claim 5, Moser in view of Sudjian teaches the limitations of claim 2.

Moser further the mutually quadrature phase shifted signals are generated by a voltage controlled oscillator (fig. 4: elements VCO, ICK and QCK).

With regards to claim 6, Moser in view of Sudjian teaches the limitations of claim 5.

Moser further teaches a frequency error signal produced by the quadricorrelator is inputted to a coarse control input of the voltage controlled oscillator (fig. 1: elements 8, 14, 6 and 2: col. 2, lines 25-30: coarse frequency lock) via a first charge pump (fig. 1: element Charge Pump) coupled to a first low-pass filter (wherein a low-pass filter is a type of loop-filter) coupled to an multiplexer (fig. 1: wherein the phase and frequency error signals are added onto the line input to element 6).

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moser (USPN 6,853,696) in view of Sudjian (US 7,409,027) as applied to claim 1 above, further in view of Morgan (USPN 6,320,406).

With regards to claim 3, Moser in view of Sudjian teaches the limitations of claim 1, including said first signal pair and second signal pair, including said phase detector.

Moser teaches the phase detector comprises a D flip-flop (fig. 2: elements 34a and 34b: col. 7, lines 50-63) receiving the first signal (fig. 2: signal FQ2: col. 7, lines 50-63) and being clocked by the second signal (fig. 2: signal FQ1: col. 7, lines 50-63), second signal being inputted to respective logic gates, including NOT and NOR gates (fig. 2: elements 34a,b, FQ3A, 36a,b and NOT gate).

Moser does not teach two Limitations: Limitation 1) the first signal pair and the second signal pair; and Limitation 2) the second signal being inputted to respective gates of a first transistors pair for determining a state ON or OFF of a current through said first transistors pair.

Limitation 1)

Sudjian teaches adapting D flip-flops (figs. 3 and 4: elements 22a-22b and 32a-32b) and multiplexers (figs. 3 and 4: elements 22a-22b and 34) to be compatible with differential incoming data signals (fig. 3: signal DATA: col. 5, lines 54-65) and differential quadrature clock signals (fig. 3: elements VCO_0 and VCO_90: col. 5, lines 54-65).

One of ordinary skill in the art at the time of the invention would clearly recognize the benefits of modifying the quadricorrelator of Moser to with the teachings and differential circuitry of Sudjian to yield the predictable benefits and results of implementing frequency detection (using a quadricorrelator) on a differential data signal as opposed to a single-end signal. Specifically, it would have been obvious to modify

the known frequency detector circuitry (Moser elements 20 and 22 which are with in the quadricorrelator) with the known differential D flip-flops and differential multiplexers of Sudjian in order to perform similar functions on a differential input data signal and differential quadrature clocking signal to generate differential error signals (where FQ1 and FQ2 are originally single-end signals), where the modified FQ2 and FQ1 are the claimed first and second signal pair, respectively, and the differential D flip-flop pairs clock by differential quadrature clock signal are obviously double edge clock bi-stable circuits, and the relationship between the phase detector (Moser: fig. 2: elements 34a and 34b) and signals FQ1 and FQ2 was previously addressed. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the quadricorrelator (frequency detector) of Moser to with the teachings and differential circuitry of Sudjian to yield the predictable benefits and results of implementing frequency detection (using a quadricorrelator) on a differential data signal as stated above.

Limitation 2)

Morgan teaches that NOT gates and NOR gates are made using transistors (fig. 11: elements 110, 1100-1101, 114, 1140-1145: col. 7, line 27 through col. 8, line 21), where the NOT gate is shown to (fig. 11: elements 1100-1101) include a transistor pair (fig. 11: elements 1100 and 1101: col. 7, lines 35-40), and that the input to the NOT is attached to the gates of the first transistor pair for determining a state ON or OFF of a current through said first transistors pair and thus implements the logical function of a NOT gate (fig. 11: elements 1100 and 1101: col. 7, line 27 through col. 8, line 21).

One of ordinary skill in the art would clearly recognize that the NOT gate of Moser includes a first transistor pair, where the input to the NOT gate is connected with the first transistors pair for determining a state ON or OFF of a current through said first transistors pair. Therefore it would have been obvious to one of orindary skill in the art at the time of the invention that the FQ1 feeding into the NOT gate of Moser in view of the teachings of transistor pairs to implement NOT gates disclosed by Morgan obviously meets the claim limitation of the second signal being inputted to respective gates of a first transistors pair for determining a state ON or OFF of a current through said first transistors pair.

Allowable Subject Matter

7. Claims 4 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 8 and 9 are allowed.

Reasons for Allowance

9. The following is a statement of reasons for the indication of allowable subject matter:

The present invention comprises Phase Locked Loop (PLL) comprising a voltage controlled oscillator (VCO) having a coarse and fine control input; a quadricorrelator generating a frequency error signal inputted to the coarse control input via first charge pump and first lowpass filter, the quadricorrelator comprising: a first and second pair of

double edge clocked bi-stable circuits coupled to multiplexers to generate a first and second signal pair, wherein said multiplexers are supplied mutually quadrature phase shifted signals from the VCO; the first and second signal pair indicative for phase difference between an incoming signal and mutually quadrature phase shifted signals; a phase detection circuit for receiving the first signal pair and being clock by the second signal pair attached to first transistor pair for determining a state ON or OFF of a current through said first transistor pairs; and a second phase detector generating phase error inputted to the fine control input of the voltage controlled oscillator via a second charge pump coupled to a second lowpass filter. The closest prior art Moser et al. (USPN 6,853,696) shows a similar system which also includes PLL with a frequency detector for mutually quadrature phase shifted signals. However, Moser et al. fails to disclose the quadricorrelator including double edge clocked bi-stable circuits, wherein the first and second signal pair is indicative of the phase difference between an incoming signal and mutually quadrature phase shifted signals and a second phase detector generating phase error inputted to the fine control input of the voltage controlled oscillator via a second charge pump coupled to a second lowpass filter. The distinct feature are contained in independent claim 8, thus rendering claims 8 and 9 allowable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES M. PEREZ whose telephone number is

(571)270-3231. The examiner can normally be reached on Monday through Friday: 9am to 5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/James M Perez/
Examiner, Art Unit 2611
5/22/2009
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611